

29/637840

1 PERIPHERAL COMPONENT INTERCONNECT ARBITER IMPLEMENTATION
2 WITH DYNAMIC PRIORITY SCHEME

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6 ABSTRACT OF THE INVENTION

7 A dynamic priority scheme is provided that uses
8 information including the status of the target and data
9 availability in deciding which PCI master should be
10 assigned ownership of the bus. The target uses delayed
11 transactions to complete a read access targeted to it. The
12 target also integrates a buffer management scheme, in one
13 embodiment an input/output cache, for buffer management.
14 The present invention optimizes the performance and
15 utilization of the PCI bus.

09637846-031000